Claims

1. An arrangement including a display device (303) and a processor (301) controlling the display device, **characterized** in that the arrangement comprises

- an intelligent display device connection interface (302) integrated in the display device,

- a memory bus (304) connected to the processor (301) in order to realize the signaling between the processor (301) and the display device connection interface (302), and

- an adapter circuit (402) in order to match the signals between the memory bus (401, 510) and the display device connection interface (404, 540).

2. An arrangement according to claim 1, **characterized** in that the intelligent connection interface of the display device is the MeSSI (Medium Speed Screen Interface) (302) manufactured by Nokia Oyj.

3. An arrangement according to claim 1, **characterized** in that the memory bus (304) connected to the processor (301) is a non-synchronized memory bus.

4. An arrangement according to claim 1, **characterized** in that the arrangement includes a memory bus (304) for realizing the signaling between the processor (301) and the memory unit (303), as well as between the processor (301) and the display device connection interface (302).

5. An arrangement according to claim 1, **characterized** in that the adapter circuit (402) includes means for synchronizing the signals (511, 512, 513, 514, 515, 516) of the memory bus (401, 510) in an order required by the display device.

6. An arrangement according to claim 1 and 5, **characterized** in that the adapter circuit (402) is provided with gates (51, 54, 57, 58, 59, 61) in order to match the signals (603, 604) between the memory bus (401, 510) and the connection interface (404, 540).

7. An arrangement according to claim 1, **characterized** in that the arrangement also includes an interference protection segment (403, 530) in order to prevent electric interference.

8. A method for connecting a display device (303) to a processor (301) controlling the display device, **characterized** in that

- in the display device (303), there is integrated an intelligent connection interface (302),
- the signaling between the processor (301) and the display device connection interface (302) is realized through a memory bus (304) connected to the processor (301), and
- the signals between the memory bus (401, 510) and the display device connection interface (404, 540) are adapted to be compatible by means of an adapter circuit (402).

9. A method according to claim 8, **characterized** in that the memory bus (304) connected to the processor (301) is arranged to function both as a bus between the processor (301) and the memory unit (303), and a bus between the processor (301) and the display device (303).

10. A method according to claim 8, **characterized** in that the adapter circuit (402) is used for synchronizing the signals (603, 604) between the memory bus (401, 510) and the display device connection interface (404, 540) to be compatible.

11. A method according to claim 8, **characterized** in that the memory bus (401) and the display device connection interface (404) are connected by glue logics together in order to achieve communication therebetween.

12. An adapter circuit display device for realizing signaling between the controlling processor (301) and the display device (303), **characterized** in that the signaling between the processor (301) and the display device connection interface (302, 404, 540) is realized through a memory bus (304, 401, 510) connected to the processor (301), and that the adapter circuit (402) electrically matches the display device connection interface (404, 540) and the memory bus (401, 510).

13. An adapter circuit according to claim 12, **characterized** in that the adapter circuit (402) is provided with gates (51, 54, 57, 58, 59, 61) for synchronizing the timing of the signals (603, 604) between the display device connection interface (404, 540) and the memory bus (401, 510), and for combining the connection interface (404, 540) and the memory bus (401, 510) as a physical, uniform bus.